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Investigation on the Short-circuit Behavior of an Aged IGBT Module Through a 6 kA/1.1 kV Non-Destructive Testing Equipment

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***Abstract* —This paper describes the design and development of a 6 kA/1.1 kV non-destructive testing system, which aims for short circuit testing of high-power IGBT modules. An ultra-low stray inductance of 37 nH is achieved in the implementation of the tester. An 100 MHz FPGA supervising unit enables 10 ns level control accuracy of the short-circuit duration, protection triggering, and acquisition of the electrical waveforms. Moreover, a protection circuit avoids explosions in case of failure, making the post-failure analysis possible. A case study has been carried out on an aged 1.7 kV IGBT power module. The case study shows the current and voltage waveforms during short-circuit, as well as the current mismatch among six inner sections, which demonstrate the capability and the effectiveness of the proposed setup in the short-circuit aspect reliability studies of MW-scale power modules.**

***Keywords*— Insulated Gate Bipolar Transistor (IGBT), Non-destructive testing (NDT), Short-circuit, Power module, Degradation.**

I. INTRODUCTION

In modern power electronics systems, there are increasing demands to improve whole system endurance and safety level while reducing manufacturing and maintenance costs [1]. According to a questionnaire for manufacturers, semiconductor devices are considered as the most critical and fragile component in industrial power electronic systems [2]. Based on another survey, semiconductor failure and soldering joint failure in power devices take up 34% of power electronic system failures [3]. Because Insulated Gate Bipolar Transistors (IGBTs) are one of the most critical components as well as the most widely used power devices in industrial power electronic systems in the range above 1 kV and 1 kW [3], the reliability of IGBTs has drawn more and more attention. In particular, for critical applications like MW-level wind turbine systems, the ability of IGBT withstanding abnormal conditions (e.g. short-circuits or overloads), is strictly required to achieve sufficient robustness for the power electronic systems [4].

For the above reasons, reliability assessment of IGBT module, especially the high-power module for MW-level application is highly demanded to prevent potential failure. IGBT failure behaviors can be classified as open-circuit failure and short-circuit failure. Generally, IGBT open-circuit failure is considered as not fatal to converters, because the converter can operate with lower quality of output with fault-tolerant control. However, short-circuit failure is critical to converters, since the uncontrolled high-level short-circuit current may destroy and even explode the failed IGBT and/or other components in the system [5]. At present, 10 μs is a typical duration stated for short-circuit withstanding capability by IGBT manufacturers. However this value does vary from one IGBT to another due to manufacturing variations and due to degradations. So far it is not definitely clear how –and how much the tolerance of the IGBT to overloads and short circuits could vary during its entire service life, which is critical for reliability design and maintenance costs estimation.

Research efforts have been devoted to the study of the short-circuit behavior of IGBTs. In [6], the short-circuit current capability is studied by repetitive low-energy-level short-circuit tests. It reveals that the short-circuit currents are reduced with testing time due to the Al metallization layer degradation and the on-state resistance increase. In [7], a "critical energy (E_C)" is proposed to explain the mechanisms of IGBT failure under repetitive short-circuit operations. When short-circuit dissipated energy is below E_C, IGBT may survive for more than 10^4 times repetitive short-circuit operations. However, when short-circuit energy is far beyond E_C, IGBT may fail after first short-circuit because of thermal runaway. A further experimental investigation show that IGBT can turn-off short-circuit successfully but fails after several microseconds when the short-circuit energy is lightly higher than E_C. It is still challenging to determine the exact value of E_C, even though many experiments and numerical simulations have been done in the prior-art research [8]. In [9], short-circuit current differences among the IGBT modules from a same production batch are investigated. However, in the prior-art studies, it is still a lack of method or setup to experimentally observe the current capability and current distribution among parallel chips of high IGBT power modules during short-circuit.

Traditional short-circuit testing circuit includes device under test (DUT), a set of capacitors and a circuit breaker in series. Over-current detection is integrated to avoid the DUT explosion, which cannot totally prevent potential damage [6]-[7]. Recently, a non-destructive testing concept has been proposed by precisely control the testing time, allowing repetitive short-circuit testing of IGBTs without catastrophically damages [10]-[11]. It is a very cost-effective way especially for testing high power IGBT modules. The implementation of non-destructive testing

systems for discrete IGBTs (up to 100 A) and for high power IGBT modules (up to 2.4 kA) are discussed in [10] and [11], respectively. The main focus of these testing systems is to study the discrete IGBTs short-circuit current behavior, which are lack of the capability to obtain short-circuit current capability of the high power IGBT modules.

In this paper, a state-of-the-art non-destructive tester (NDT) is proposed with the capability of 6 kA/1.1 kV electrical acquisitions during IGBTs short-circuit which is appropriate for high-power IGBT modules. A Field-Programmable Gate Array (FPGA) based controller supplies 10 ns precise short-circuit time control and corresponding accurate electrical measurement. With the advanced busbar design by Q3D simulations [13], an ultra-low total circuit stray inductance of 37 nH is achieved in the NDT implementation. To demonstrate the capability and performance of the developed testing system, a case study on the short-circuit behaviors of an aged high power IGBT module is presented. The paper is organized as follows: Section II describes the principle and implementation of the NDT, including low inductance busbar design, FPGA based timings setting. Section III presents the case study of an aged 1.7 kV/1 kA IGBT module. It evidently demonstrates the capability of the testing system in investigating the electrical behaviors during short-circuits by accurate timing control and detecting uneven current distribution among several sections of the power modules. Section V concludes the paper with discussions.

II. Description of the Non-destructive Testing System

2.1 Structure and Operating Principle

The basic idea of non-destructive testing is performing repetitive short-circuit tests without destroying IGBTs. It is challenging because both high voltage and high current are applied at IGBTs during short-circuits. The power shock can damage IGBT within several µs. Therefore, the Non-Destructive Testing (NDT) is constructed in the lab, the picture and circuit of which are as shown in Fig.1 and Fig. 2.

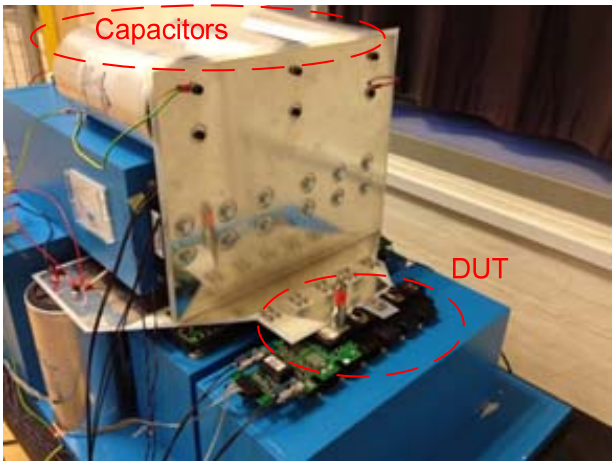


Fig. 1. Picture of the Non-Destructive Testing setup using the power circuit in Fig. 2.

The NDT structure includes the following parts. A high-voltage power supply charges up a high-voltage capacitor bank C_{DC}. The stored energy is used to supply for short-circuits. The on-state series protection switch will be switched off immediately after the test and save the DUT. A Computer-Aided-Design (CAD) busbar has been developed to minimize the overall circuit inductance, including the intrinsic inductances of the series protection and the capacitors. It is achieved by optimization of the mutual coupling of the busbar components. A 100 MHz FPGA provides the driving signals for the DUT and the switches for the protection, and also provides the precise time control for electrical measurement. The remote control and data acquisition is achieved by a Personal Computer (PC) which supervises the operation by connecting a LeCroy HDO6054-MS oscilloscope via an Ethernet link and a FPGA board through an RS-232 bus. Two commercial IGBT drivers drive the protection switches and the DUT respectively. In order to perform short-circuits, the corresponding protection circuit on the DUT drivers has been deactivated. During tests, collector current, collector voltage and gate voltage waveforms are acquired together with the current flowing through a specific section of the DUT.

Fig. 1 shows a photograph of the laboratory setup, where the dimension is around 1 m x 1 m x 1 m. The electrical schematic of the NDT with the commutation Loop 1 and Loop 2 is shown in Fig. 2. It includes the DUT, the series protection, parallel protection, load inductance L_{load}, DC link capacitance C_{DC}, a high voltage power supply V_{DC}, Schottky diodes, negative-voltage capacitance C_{NEG} with corresponding negative voltage supply V_{NEG}.

The operating principle is as follows: as shown in Fig. 2, the power circuit is divided into two loops – Loop 1, (the main loop in the Table I) including the series protection, and Loop 2, including a parallel protection; the DUT is located in the common branch. Table I gives the specifications of major components in Fig.2. The tester is operated in a standard single-shot way, so that the energy stored in the capacitors C_{DC} is used for the tests. C_{DC} and C_{NEG} are composed of five and three capacitors in parallel, respectively, in order to reduce the intrinsic stray inductances. The same principle has been adopted for the two switches of the series protection, the two switches of the

TABLE I. The Specifications and Main Components Applied in the Power Circuit Parameters.

haracteristic	Value
Maximum voltage	1.1 kV
Maximum current	6 kA
C_{DC} capacitors	5 x 1100 µF
Stray inductance of the main loop	37 nH
Devices in series protection	2 x Dynex DIM1500ESM33-TS000, 3 kA, 3.3 kV
Devices in parallel protection	2 x Mitsubishi CM1200HC-66H 2.4 kA, 3.3 kV
C_{NEG} capacitors	3 x 1100 µF
Schottky diodes	5 x 170 V, 1.2 kA

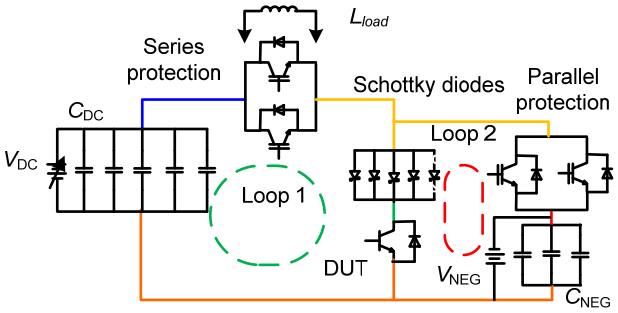


Fig. 2. Detailed schematic of the power circuit of the Non-Destructive Tester.

parallel protection and the five Schottky diodes.

Loop 2 is designed to improve the performance of the NDT. The "non-destructive testing" means that the series protection is activated right after the commutation to prevent the DUT from explosions in case of failure. This capability is strictly dependent on the series protection's capability to cut the current flowing through the DUT to zero immediately after the test. However, the turn-off transition of the series protection is non-ideal because IGBT switches have current tails, which would continue flowing through the DUT. To avoid this effect and divert the current tail, the parallel protection is fired up together with the activation of the series one. As demonstrated in [12], to improve the parallel intervention as well, a negative voltage biases a capacitor bank C_{NEG} in order to enhance the voltage fall promptness during IGBT turn-on. Furthermore, to avoid a negative current flowing through the DUT, the Schottky diode bank is placed in series.

There are two different short-circuit types: Type 1 short-circuit happens during the IGBT turn-on, while Type 2 short-circuit happens when the IGBT is at on-state, as illustrated in Fig. 3. The NDT can provide both short-circuit types by different configuration and control timing schemes. Control timing schemes for the two types short-circuit will be further illustrated in Section II, Part 3.

2.2 Low Inductance Busbar Layout

The high current slope during turn-on and turn-off short-circuits (at kA/us level) can cause voltage spikes, thus the stray inductance should be controlled at a very low level (at nH). The busbar design of the NDT power circuit is

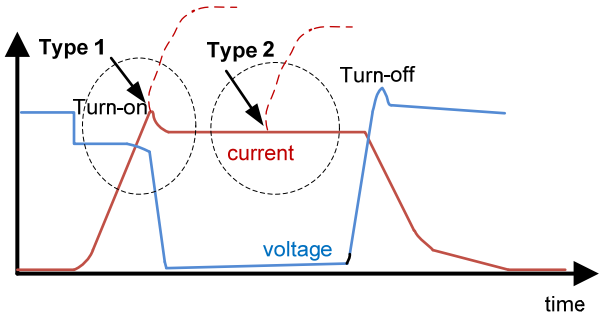


Fig. 3. Two types of short-circuits: Type 1 occurs during turn-on, Type 2 occurs during conduction state.

illustrated in Fig. 4. Fig. 4 (a) provides a 3D view of the NDT: the DUT is the black module in the lower right corner, and the two capacitor arrays C_{DC} (5x) and C_{NEG} (3x) are located under busbar. Parallel and series protection are also behind the busbar. Schottky diodes are mounted in five square windows close to the DUT. Colors adopted for the busbar layers are coherent among Figs. 2, 4 (a) and 4 (b). An original upside-down-T-shaped busbar is adopted, as illustrated in Fig. 4 (b). The cross section of the whole busbar system has been reported, together with some blocks indicating the main components of the circuit. The adopted geometry allows observing the DUT behaviors by measuring equipment during the commutations.

Short-circuit tests by the manufacturer is normally performed without series protection, in order to keep the circuit total inductance at an acceptably low value. The presence of the series protection in the NDT main loop increases the circuit stray inductance. Therefore, the design of a low inductance busbar is becoming more critical for the

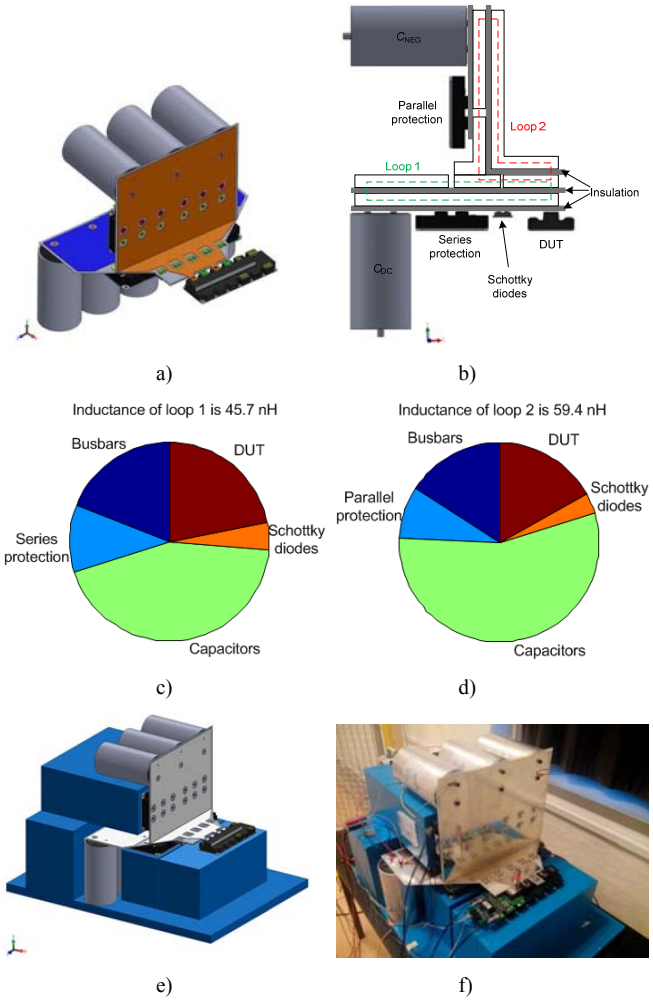


Fig. 4. Busbar design of the power circuit: a) 3D view of the core of the NDT setup including the busbar; b) principle cross-section of the busbar layers: Loop 1 is the horizontal one, Loop 2 is the vertical one (see Fig. 2); c) Ansys Q3D simulated distribution of the Loop 1 inductance and d) of the Loop 2 inductance; e) virtual prototype of the NDT setup; f) physical prototype of the NDT setup.

NDT.

The design of the NDT busbar has been performed with 3D FEM modelling tool. Ansys Q3D [13] simulation outputs have been reported in Figs. 4 (c) and 4 (d), respectively for Loop 1 and Loop 2. Finally, Figs. 4 (e) and 4 (f) illustrate the whole power circuit design and the picture of the constructed setup, respectively. Based on the Q3D simulations, the calculated equivalent stray inductances of the Loop 1 busbar is 8.6 nH, and the inductance of the Loop 2 busbar is estimated to be 9.4 nH. According to the datasheets, parasitic inductance of the DUT, the Schottky diode, the DC capacitor, the series protection, and the parallel protection, are 10 nH, 10 nH, 100 nH (maximum value), 10 nH, and 10 nH, respectively [14]-[16]. Therefore, the total inductances of the commutation Loop 1 and Loop 2 are 45.7 nH and 59.4 nH, respectively, as shown in Figs. 4 (c) and 4 (d). These low inductance values are achieved by the placement of the components in a way with negative mutual coupling among them and by the application of a 200 µm Mylar isolation foil for the busbar.

The low stray-inductance design is verified by experimental switching waveforms as shown in Fig. 5. It can be noted that the peak value of V_{CE} is 1253 V and the DC voltage is 900 V. The current is decreased linearly by 351.9 A in 36.8 ns. Therefore, the obtained stray inductance of Loop 1 is:

$$L_{Loop1} = \frac{(1253V - 900V) \times 36.8ns}{351.9A} = 37nH \quad (1)$$

It implies that the simulation result is relatively conservative compared to the experimental one (i.e., 81 % of the simulated value). It is worth noting that the value of 37 nH includes intrinsic inductance of the IGBT modules for series protection and the capacitor bank C_{DC}. The 19 % difference compared to the simulation result is mainly due to the parasitic inductance in the capacitor. In the simulation, the maximum value of 100 nH of each capacitor in the datasheet is used, while the measured inductance of each capacitor is 40 nH.

2.3 FPGA Operation Timings Setting

As discussed in section 2.1, short-circuits are classified as Type 1 and Type 2, as illustrated in Fig. 3. The circuit configuration and control timing schemes for the two types

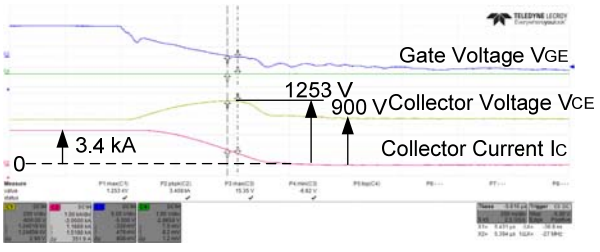
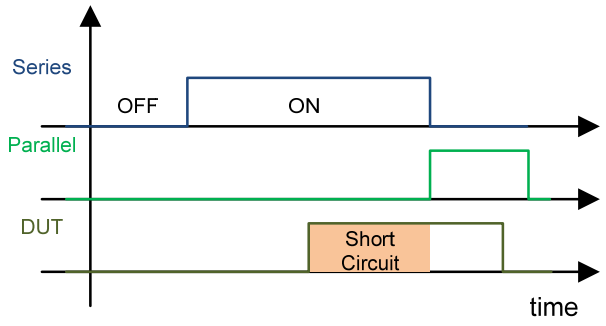


Fig.5. Experimental waveforms of short-circuit turn-off used for measuring the busbar total inductance.

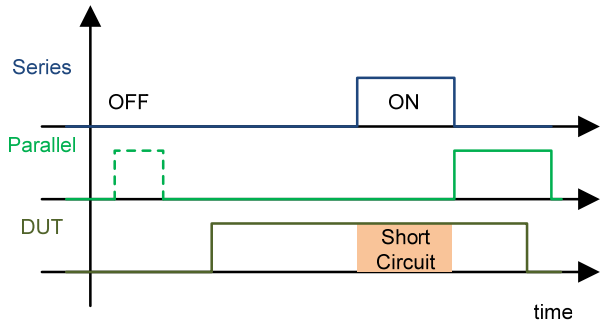
short-circuit are illustrated as follows:

For Type 1 short-circuit which happens at the device turn-on transient, the load inductance L_{load} is removed. Before tests, the series protection is in on-state and the parallel protection is off-state. Loop 1 has the stray inductance only and the Schottky diodes behave almost ideally, so the DUT is connected directly to the C_{DC} capacitors. During the tests, the DUT falls to short-circuit when it is triggered. After the precise controlled time by 100 MHz FPGA, the DUT short-circuit is switched off by series protection IGBTs. At the same time, the parallel protection is turned on to avoid the undesirable tail current through DUT. The corresponding control time sequences of the series and parallel protections and DUT are as shown in Fig. 6 (a). The negative voltage V_{NEG} can speed up the parallel protection, and the Schottky diodes can avoid a current flow from the DUT to the negative voltage.

Type 2 short-circuit happens during on-state of the device, and the load inductance L_{load} is required to obtain high current. At first, the series protection is off-state while DUT is turned on. The series protection diodes operate as freewheeling for the load inductance. In this case, the current flowing through the DUT is determined by the load inductance. Then, the series protection is turned on and triggered by an on-state short-circuit to DUT. Finally, short-circuit is ended with series protection turned off and parallel protection turned-on. The corresponding control time sequences of series, parallel protections and DUT are as

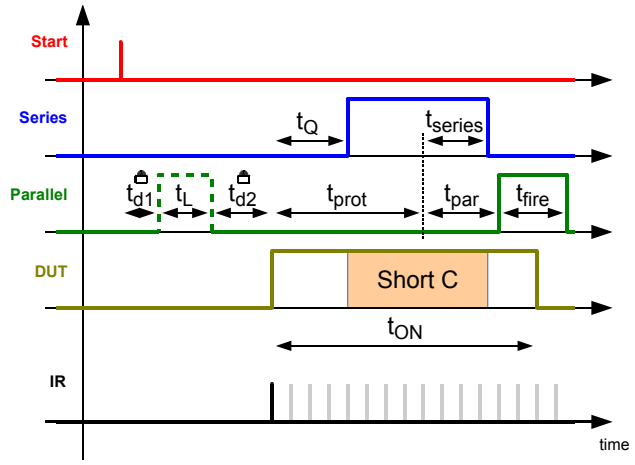


a)

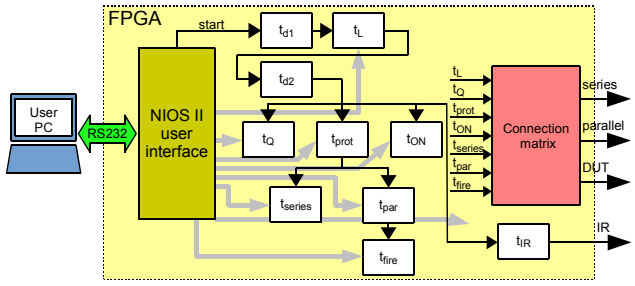


b)

Fig. 6. Timing settings for two types short-circuits: a) Timing diagram for Type 1 short-circuit; b) Timing diagram for Type 2 short-circuit.



a)



b)

Fig. 7. FPGA controller settings: a) Operation timings of the proposed apparatus; b) implementation of the time sequencer in FPGA.

shown in Fig. 6 (b).

The above timings are achieved by an FPGA-based supervising unit, as illustrated in Fig. 7. It can be recognized that the timings shown in Fig. 6 (a) and 6 (b) can be obtained by a proper choice of the timing shown in Fig. 7 (a). Through defining the series protection delaying timings - t_Q and t_{prot}, as well as the on-state timing t_{series}, the starting point and duration of series protection can be controlled. In a similar way, the parallel protection starting point and duration can be achieved through the parallel delaying timing t_{par} and on-state timing t_{fire} and t_L. DUT on-state duration can be obtained by the on-state timing t_{ON}. The delaying timings – t_{d1} and t_{d2} are normally locked to avoid undesired devices short-circuit. A development board DE2-115 from Terasic Corp [18] hosting an ALTERA Cyclone IV FPGA [19] is used to implement the supervising unit of the testing apparatus. Its principle schematic is shown in Fig. 7 (b). A NIOS II embedded processor is used to interface the user with the timing sequencer via an RS-232 standard bus. The timing sequencer is made up of several timers (white blocks in Fig. 7 (b)) which have been concatenated in the shown way in order to produce the sequence and the implications of Fig. 7 (a). The whole timing sequence is initiated by the start signal (upper left) generated by the FPGA processor as well. A connection matrix is put at the right end of the supervising unit to combine the signals from left-side timers to produce the four main outputs. Such outputs are fed to a hardware interface, which drives the

TABLE II. MAIN SPECIFICATIONS OF IGBT MODULE UNDER TEST.

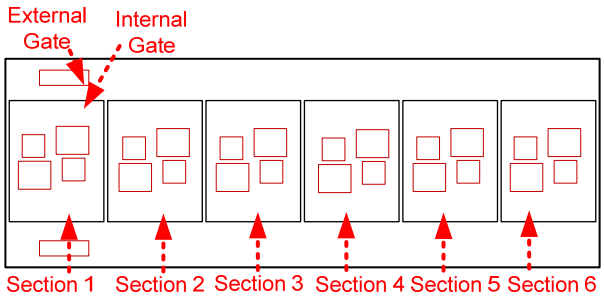
Characteristic	Value
Collector-emitter voltage V_{CES}	1.7 kV
Continuous DC collector current I_{Cnom}	1 kA
Rated short-circuit current I_{SC}	4 kA
Gate-emitter maximum voltage V_{GES}	+/- 20V
Internal gate resistance	0 Ω
Number of parallel sections	6

DUT, series protection and parallel protection, all of which are IGBT devices, in the NDT through optic fibers. The above supervising unit is driven by an 100 MHz oscillator to achieve a time resolution of 10 ns. Each timer is 32 bits wide, so that a maximum time of more than 40 second can be achieved for each delay in Fig. 7 (a).

III. CASE STUDY ON THE SHORT-CIRCUIT BEHAVIOR OF AN AGED 1.7 KV/1 KA IGBT MODULE

3.1 Information on the DUT

The developed testing system has been utilized to study the short-circuit behaviors of a 1.7 kV/1 kA IGBT module, which e.g. is widely used in wind turbine systems. The main specifications are summarized in Table II. It is noted that rated short-circuit current is 4 kA. As shown in Fig. 8 (a), there are six sections connected in parallel to increase the current capability. The external gate represents the IGBT module gate terminals, and the internal gate represents the location near the chip gate bond-wire. Each section contains two IGBT chips and two freewheeling diode chips, which are configured as half-bridge. The module is mounted into the NDT system, as shown in Fig. 8 (b), which enables



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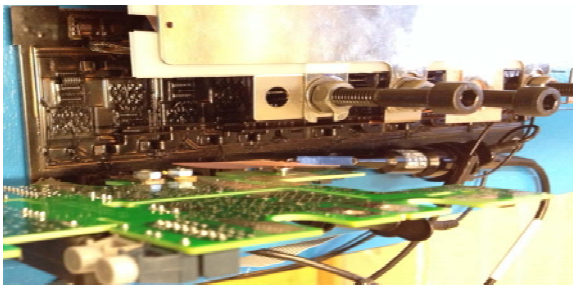

b)

Fig. 8. Information of studied 1.7 kV/1 kA IGBT power modules: a) Geometry of the internal structure, section 1 is closet to gate leads while section 6 is farthest to the gate leads, b) module connected to the busbar.

current measurement of the six sections independently by means of a Rogowski coil.

As mentioned before, the short-circuit tolerance ability of aged IGBT module is critical for reliability design and maintenance costs. Meanwhile, it is not explicitly known the short-circuit current distribution among different IGBT chips inside the IGBT module. In this case study, an aged IGBT module is investigated.

3.2 Electrical Acquisitions of the studied IGBT Module

At first, the IGBT module is tested under 500 V for 1.2 µs short circuit at room temperature (25°C), the peak short-circuit current reaches 2 kA. Gate voltage (V_G) waveform during test is plotted in Fig. 9 (a). The collector current (I_C) and the collector-emitter voltage (V_{CE}) waveforms during short-circuit are shown in Fig. 9 (b). The collector voltage drop during short-circuit turn-on and voltage peak during short-circuit turn-off is due to the stray inductance and high current slope d*i*/d*t*.

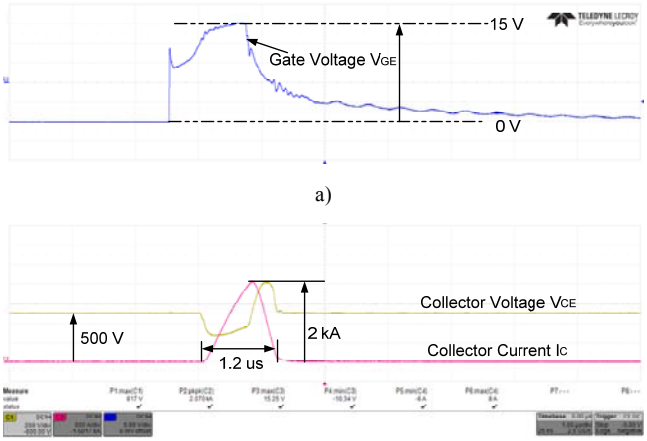

Fig. 9. Electrical behavior during a 500 V/2 kA/1.2 µs short-circuit: a) external gate voltage waveform (5 V/div), b) collector voltage and current waveforms (200 V/div; 500 A/div; 1 µs/div).

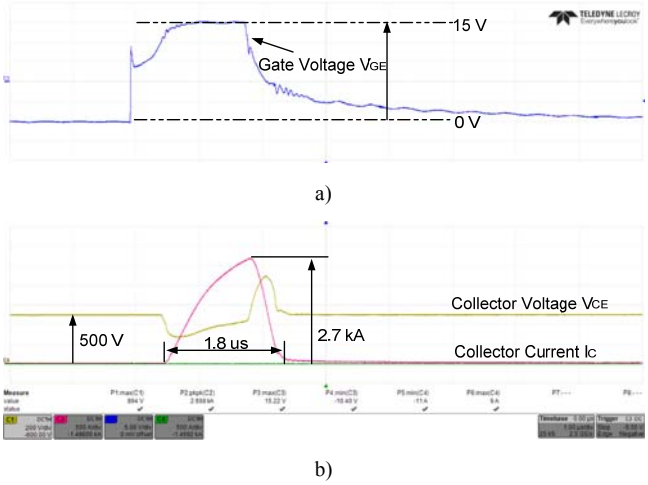

Fig. 10. Electrical behavior during a 500 V/2.7 kA/1.8 µs short-circuit: a) external gate voltage waveform (5 V/div); b) collector voltage and current waveforms (200 V/div; 500 A/div; 1 µs/div).

Through slightly increasing the short-circuit duration time by the advanced FPGA controller, DUT is tested for 1.8 µs short circuit at 500 V room temperature (25°C). Short-circuit current increases to 2.7 kA. Fig. 10 (a) shows the external gate voltage waveform and Fig. 10 (b) shows the collector current and voltage waveforms during short-circuit. Owing to the FPGA controller, the short-circuit time duration could be increased or decreased with a step of 10 ns, which provides possibility of comprehensively investigating IGBT module short-circuit behaviours.

With the power supply voltage rising, DUT is tested under 900 V for 5 µs short circuit at room temperature (25 °C). Short-circuit current reaches the saturation value -3.5 kA. Fig. 11 (a) shows the collector current and voltage waveforms during short-circuit. It is evidenced that the collector voltage maintains DC voltage (900 V in Fig. 11 (b) during short-circuit. It clearly shows the I_C is lower than the rated short-circuit current (4 kA), which may be due to the degradation in the solder layer under IGBT chips. Further investigations on module solder layer conditions should be carried out in future.

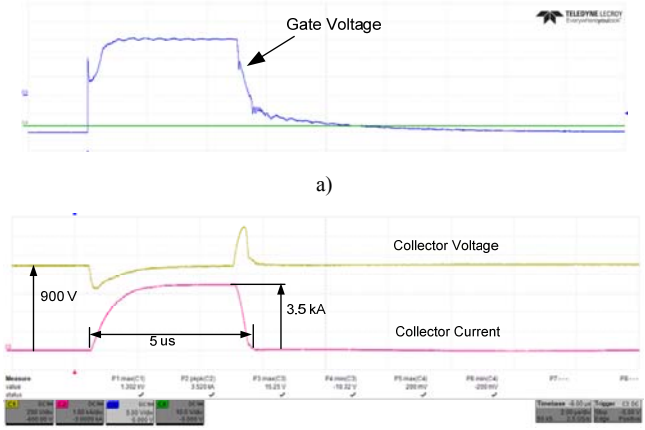

Fig. 11. Electrical behavior during a 900 V/3.5 kA/5 µs short-circuit: a) external gate voltage waveform (5 V/div); b) collector voltage and current waveforms (200 V/div; 1 kA/div; 2 µs/div).

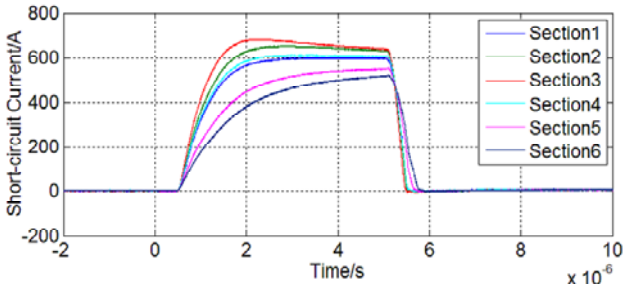

Fig. 12. Short circuit current distribution among 6 sections at the same test conditions of Fig. 8. Lower short-circuit currents flow at farther sections from the external gate.

3.3 Acquisitions of Short-circuit Current Distribution inside the IGBT Module.

In order to further investigate the current distribution among the six sections inside the aged IGBT module, short-circuit tests under 900 V for 5 μs have been carried out repetitively. The current of each section can be measured by means of a Rogowski coil probe.

Short-circuit current waveforms are plotted in Fig. 12 under the same test conditions of Fig. 11. The section number is consistent with numbers in Fig. 8 (a). It evidences highly imbalanced short-current currents among six sections. The imbalance of current amplitude and turn-on slopes among the six sections, clearly evidences the ageing effects on short-circuit capability. It is worth mentioning that the imbalance is not related to the section position, i.e., stray inductance. For instance, section 1 is the closest to the external gate leads; however the current amplitude is not the highest, as shown in Fig. 12. The above phenomenon shows short-circuit performances are significantly affected by ageing, thus reversely reducing IGBT module expected performance in terms of short-circuit withstanding capability.

V. CONCLUSIONS

A 6 kA/1.1 kV non-destructive-testing equipment for high power IGBT modules short-circuit tests has been developed, which adopts FEM simulations for optimizing the busbar layout to achieve total circuit inductance at 37 nH. A 100 MHz FPGA with a custom sequencing circuit operating together with an embedded microprocessor is used to finely coordinate the testing operations.

Its capabilities have been used to study the electrical behavior of an aged 1.7 kV/1 kA IGBT module under short circuit conditions. Uneven current sharing among different sections has been found in this aged module.

Moreover, with the non-destructive approach a large amount of reproducible measurements can be acquired without any catastrophic damage. In any case, the intrinsic energy limitation owing to the protection circuit avoids device explosion, which provides the critical prerequisite for post-failure analysis.

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